Dual non-retriggerable monostable multivibrator with reset

74HC/HCT221

FEATURES

- Pulse width variance is typically less than ± 5%
- Pin-out identical to “123”
- Overriding reset terminates output pulse
- nB inputs have hysteresis for improved noise immunity
- Output capability: standard (except for nR_{EXT}/C_{EXT})
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT221 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT221 are dual non-retriggerable monostable multivibrators. Each multivibrator features an active LOW-going edge input ($n\overline{A}$) and an active HIGH-going edge input (nB), either of which can be used as an enable input.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry for the nB inputs allow jitter-free triggering from inputs with slow transition rates, providing the circuit with excellent noise immunity.

Once triggered, the outputs (nQ, $n\overline{Q}$) are independent of further transitions of $n\overline{A}$ and nB inputs and are a function of the timing components. The output pulses can be terminated by the overriding active LOW reset inputs ($n\overline{R}_D$). Input pulses may be of any duration relative to the output pulse.

Pulse width stability is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications pulse stability will only be limited by the accuracy of the external timing components.

The output pulse width is defined by the following relationship:

$t_W = C_{EXT}R_{EXT}ln_2$
$t_W = 0.7C_{EXT}R_{EXT}$

Pin assignments for the “221” are identical to those of the “123” so that the “221” can be substituted for those products in systems not using the retrigger by merely changing the value of R_{EXT} and/or C_{EXT}.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
	propagation delay	C_L = 15 pF; V_{CC} = 5 V; R_{EXT} = 5 kΩ; C_{EXT} = 0 pF			
t_{PHL}	$n\overline{A}$, nB, $n\overline{R}_D$ to nQ, $n\overline{Q}$		29	32	ns
t_{PLH}	$n\overline{A}$, nB, $n\overline{R}_D$ to nQ, $n\overline{Q}$		35	36	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1 and 2	90	96	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) + 0.33 \times C_{EXT} \times V_{CC}^2 \times f_o + D \times 28 \times V_{CC}$ where:

   f_i = input frequency in MHz; f_o = output frequency in MHz

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   C_{EXT} = timing capacitance in pF; C_L = output load capacitance in pF

   V_{CC} = supply voltage in V; D = duty factor in %

2. For HC the condition is V_I = GND to V_{CC}

   For HCT the condition is V_I = GND to V_{CC} – 1.5 V

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard (except for nR_{EXT}/C_{EXT})
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.
To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nB	0.30
$n\overline{A}$	0.50
$n\overline{R}_D$	0.50

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min	typ	max	min	max.	min.	max.			
t_{PLH}	propagation delay (trigger) n$\overline{A}$, n$\overline{R}_D$ to nQ		30	50		63		75	ns	4.5	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; Fig.10
t_{PLH}	propagation delay (trigger) nB to nQ		24	42		53		63	ns	4.5	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; Fig.10
t_{PHL}	propagation delay (trigger) n$\overline{A}$ to n$\overline{Q}$		26	44		55		66	ns	4.5	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; Fig.10
t_{PHL}	propagation delay (trigger) nB to n$\overline{Q}$		21	35		44		53	ns	4.5	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; Fig.10
t_{PHL}	propagation delay (trigger) n$\overline{R}_D$ to n$\overline{Q}$		26	43		54		65	ns	4.5	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; Fig.10
t_{PHL}	propagation delay (reset) n$\overline{R}_D$ to nQ		26	43		54		65	ns	4.5	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; Fig.11
t_{PLH}	propagation delay (reset) n$\overline{R}_D$ to n$\overline{Q}$		31	51		64		77	ns	4.5	C_{EXT} = 0 pF; R_{EXT} = 5 kΩ; Fig.11
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.10
t_W	trigger pulse width n$\overline{A}$ = LOW	20	13		25		30		ns	4.5	Fig.10
t_W	trigger pulse width nB = HIGH	20	13		25		30		ns	4.5	Fig.10
t_W	pulse width n$\overline{R}_D$ = LOW	22	13		28		33		ns	4.5	Fig.8
t_W	output pulse width n$\overline{Q}$ = LOW nQ = HIGH	630	700	770	602	798	595	805	µs	5.0	C_{EXT} = 100 nF; R_{EXT} = 10 kΩ; Fig.10
t_W	trigger pulse width nQ or n$\overline{Q}$		140		–		–		ns	4.5	C_{EXT} = 28 pF; R_{EXT} = 2 kΩ; Fig.10
t_W	trigger pulse width nQ or n$\overline{Q}$		1.5		–		–		µs	4.5	C_{EXT} = 1 nF; R_{EXT} = 2 kΩ; Fig.10

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min	typ	max	min	max.	min.	max.			
t_W	trigger pulse width nQ or $n\overline{Q}$		7		–		–		µs	4.5	C_{EXT} = 1 nF; R_{EXT} = 10 kΩ; Fig.10
t_{rem}	removal time $n\overline{R}_D$ to $n\overline{A}$ or nB	20	12		25		30		ns	4.5	Fig.9
R_{EXT}	external timing resistor	2		1000	–		–		kΩ	5.0	Fig.13
C_{EXT}	external timing capacitor	no limits							pF	5.0	Fig.13